

PA-DC

QUERY CONTROL FORM		RTIS USE ONLY	
Application No.	001876290	Prepared by	ACTark
Examiner-GAO	Thomas J. O'Leary	Date	4/5/04
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JACKET					
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449		
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b		
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract		
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs		
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other		

SPECIFICATION	MESSAGE
a. Page Missing	① Claim 11 depends on itself claim 11.
b. Text Continuity	② PTO-1449: Please either initial or line through citations. Copy provided.
c. Holes through Data	
d. Other Missing Text	
e. Illegible Text	
f. Duplicate Text	
g. Brief Description	
h. Sequence Listing	
i. Appendix	
j. Amendments	
k. Other	
CLAIMS	
a. Claim(s) Missing	
b. Improper Dependency	initials JC
c. Duplicate Numbers	
d. Incorrect Numbering	
e. Index Disagrees	
f. Punctuation	
g. Amendments	
h. Bracketing	
i. Missing Text	
j. Duplicate Text	
k. Other	
RESPONSE	The Examiner was authorized by Applicant's representative, Gary Hargrave (Reg. No. 20,250) to make the appropriate change to claim 11. The change is reflected by a copy of the claim included herein.
	The Examiner also initialed the IDS copy filed January 12, 2004.

50 Ωcm, and said source, drain, and their extensions are made of p-type silicon.

9. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type has a dopant species selected from a group consisting of arsenic, phosphorus, antimony, bismuth, and lithium, while said source, drain, their extensions, and said regions of higher resistivity within said semiconductor of the first conductivity type have a dopant species selected from a group consisting of boron, aluminum, gallium, indium, and lithium.

10. The circuit according to Claim 1 wherein said gate has a narrow dimension smaller than about 0.2 μm.

11. The circuit according to Claim ~~11~~¹ wherein said regions of higher resistivity enhance the gain of the lateral bipolar transistor and thus the ESD protection of said MOS transistor, especially the current needed for initiating thermal breakdown, without decreasing latch-up robustness or increasing inadvertent substrate current-induced body biasing of neighboring transistors.

12. A method of increasing the p-type semiconductor resistivity in selected regions under the active area of a NMOS transistor, said regions stretching laterally between the inner borders of the extended and recessed regions of source and drain, respectively, and vertically from a depth just below the deletion regions of said source and drain to approximately the top of the channel stop region, comprising the steps of:
25 depositing a photoresist layer over said transistor and opening a window in said layer over said

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